IN THE SPECIFICATION:

Please amend page 3, last paragraph as follows:

In the calculation of the branch target address 314, the lowest 2 bits are set to "00" (a constant value), and the next 12-bit to the lowest 2 bits portion accommodates operand portion 403 in the instruction word 312 is set as is. For the next 18-bit portion, the sum of the 18-bit sign-extended value 313 of operand portion 402 in the instruction word 312 and the PC value 311 is calculated in an 18-bit adder 321 and outputted.

Please amend page 11, last paragraph as follows:

If the op code 201 in the instruction word 511 indicates a PC+disp branch instruction, the lower bits in the instruction word 511 (equivalent to 203) and the lower 11-bit portion of the address 512 are summed in an adder 521 as an 11-bit result 513, and the selector 523 outputs the 11-bit result 513. This result is stored in the portion corresponding to the lower bits 203 in entry 514 in the instruction cache 501. The carry bit, i.e. the uppermost bit of the addition result executed by the adder 521 is stored in field 515.